## Remarks

This amendment responds to the office action mailed October 22, 2004. In the office action the Examiner:

- rejected claims 30-48 under judicially created doctrine of obviousness-type double patenting over claims 1-29 of U.S. Patent 6,163,178.
- rejected claims 49-79 under 35 U.S.C. 112, second paragraph, as being indefinite;
- rejected claims 49-51, 54 and 56-58 under 35 U.S.C. 102(b) as anticipated by Taylor et al. (USP 5,182,467);
- rejected claims 55 and 59 under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. (USP 5,182,467);
- rejected claims 64-66 and 69-75 under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. (USP 5,182,467) in view of Sugibayashi (USP 5,373,477); and
- indicated that claims 52, 53, 60-63, 67, 68 and 76-78 would be allowable if rewritten in independent form.

After entry of this amendment, the pending claims are: claims 30-79.

### Amendment

Applicants have also corrected several typographical errors appearing in claims 30-79. No new matters have been added.

### Double Patenting Rejection

A terminal disclaimer is filed herewith to address the double patenting rejection.

### Claim Rejections – 35 USC §112

Applicants have amended claims 49 and 64 by replacing the term "device" with the term "multiplexor", respectively, so as to refer to the term "[a] multiplexor" appearing previously in claims 49 and 64. Therefore, Applicants respectfully request that the rejection of claims 49-79 under 35 USC §112, second paragraph, be withdrawn.

Claim Rejections – 35 USC §102

The Examiner rejected claims 49-51, 54 and 56-58 under 35 U.S.C. 102(b) as anticipated by Taylor et al. Applicants respectfully disagree.

The predriver element of claim 49 was rewritten to provide correct antecedent references to the multiplexor element. The output driver element of claim 49 was rewritten to clarify the meaning of "a plurality of transistor stacks."

The transistors in Figure 7 of Taylor identified by the Examiner as a plurality of transistor stacks are located in a differential amplifier, and furthermore the sole purpose of differential amplifier identified by the Examiner is to bias (i.e., set the current level) of another differential amplifier at the left edge of Figure 7 of Taylor. Taylor does not provide an output driver having a plurality of transistor stacks coupled in parallel to a data signal output of the output driver.

In addition, the "predriver" element of claim 49 does not read on the "crossing amplitude buffer" of Taylor, nor is the Taylor buffer equivalent. As described in Taylor with respect to Figure 3, Taylor accomplishes duty cycle adjustment by adding an offset voltage between the single-ended components of the clock signal CLOCK2 from the divider block 15, thus changing the duty cycle to compensate for a type of timing error. None of the Taylor circuits ***adjust*** a slew rate of a data signal. While the Taylor circuit produces a signal, which inherently has a slew rate, the Taylor circuit provides no mechanism for adjusting that slew rate, and therefore the Taylor patent does not teach or suggest the predriver element of claim 49.

Since Taylor does not teach at least the features of the predriver and output driver elements in claim 49, claim 49 and its dependent claims 50, 51, 54 and 56-58 are not anticipated by Taylor.

Claim Rejections – 35 USC §103

The Examiner rejected claims 55 and 59 for being unpatentable over Taylor. In order to establish prima facie obviousness, the prior art, alone or in combination, must teach or suggest each and every limitation of the rejected claims. However, since Taylor does not teach at least the features of predriver and output driver recited in claim 49 (see the previous section), claims 55 and 59, being dependent from claim 49 are patentable over Taylor.

Claim 64 includes three elements (the multiplexor, the predriver and the output driver) also found in claim 49. Claim 64 also includes a feature that is not recited in claim 49, a charge compensation circuit.

As explained above, Taylor does not teach or suggest the predriver and output driver elements of claims 49 and 64. Furthermore, Sugibayashi (5,373,477) does not teach a predriver with slew rate adjustment, nor does it teach an output driver having transistor stacks connected in parallel to a data signal output of the output driver. Thus, the combined teachings of Taylor and Sugibayashi do not teach or suggest an integrated circuit device having the predriver and output driver elements of claims 49 and 64, and therefore claim 64 and its dependent claims are patentable over the combined teachings of Taylor and Sugibayashi.

In addition, claim 64 requires that a charge compensation circuit provide "an amount of charge ... in accordance with a charge compensation value." Neither the voltage detecting circuit 12e of Sugibayashi nor a combination of Taylor and Sugibayashi meet this requirement of claim 64. For this additional reason, claim 64 and its dependent claims are patentable over the combined teachings of Taylor and Sugibayashi.

The Commissioner is authorized to charge the required fees, under 37 C.F.R. § 1.17, and any required extension of time fees throughout the pendency of this application, or credit any overpayment, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order number 060809-0147-US).

Respectfully submitted,

Date: February 1, 2005

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